Synopsis V1.0
Single Event Latchup Testing of the
PCA80C552 Phillips Processor

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I. Introduction

This study was undertaken to determine the latchup susceptibility of the PCA80C552 Phillips Processor. The device was monitored for latchup induced high power supply currents by exposing it to a number of heavy ion beams at the Brookhaven National Laboratory Single Event Effects Test Facility.

II. Devices Tested

Devices were manufactured by Phillips. All devices were characterized prior to exposure. One device was used in this testing (only one of four parts available survived the de-lidding process as the parts were plastic encapsulated and had a polyamide layer between the die and plastic). All devices were from date code 9707.

III. Test Facility

Facility: Brookhaven National Laboratory Single Event Effects Test Facility
Flux: 1.55 x 10^2 to 5.22 x 10^4 particles/cm^2/s.

Ion	LET ($MeVcm^2/mg$)
F	3.3
Si	7.88
Cl	11.4
Ni	26.2

IV. Test Methods

Figure 1 contains a block diagram for the test configuration for the PCA80C522 processor. Power is supplied (+5 Volts) to the processor via a current monitor so that higher than nominal latch current can be observed and the device under test (DUT) protected against. A function generator is used on the Reset line of the processor to allow the processor to be reset to normal operation after a Single Event Functional Interrupt (SEFI) would occur (that was not induced via a latchup). A 16 MHz crystal supplies the required clock signal for the processor and all processor data outputs are tied to ground via a 100 kΩ resistor. Finally, a temperature control and monitoring system were in place to operate the part in the worst case condition for latchup (100 °C). However, during initial testing of the processor, no stable operation of the processor was seen after the temperature was raised above approximately 60 °C. Since testing at the standard elevated temperature was not an option, the temperature control and monitoring system was used to maintain the device at nominal room temperature.

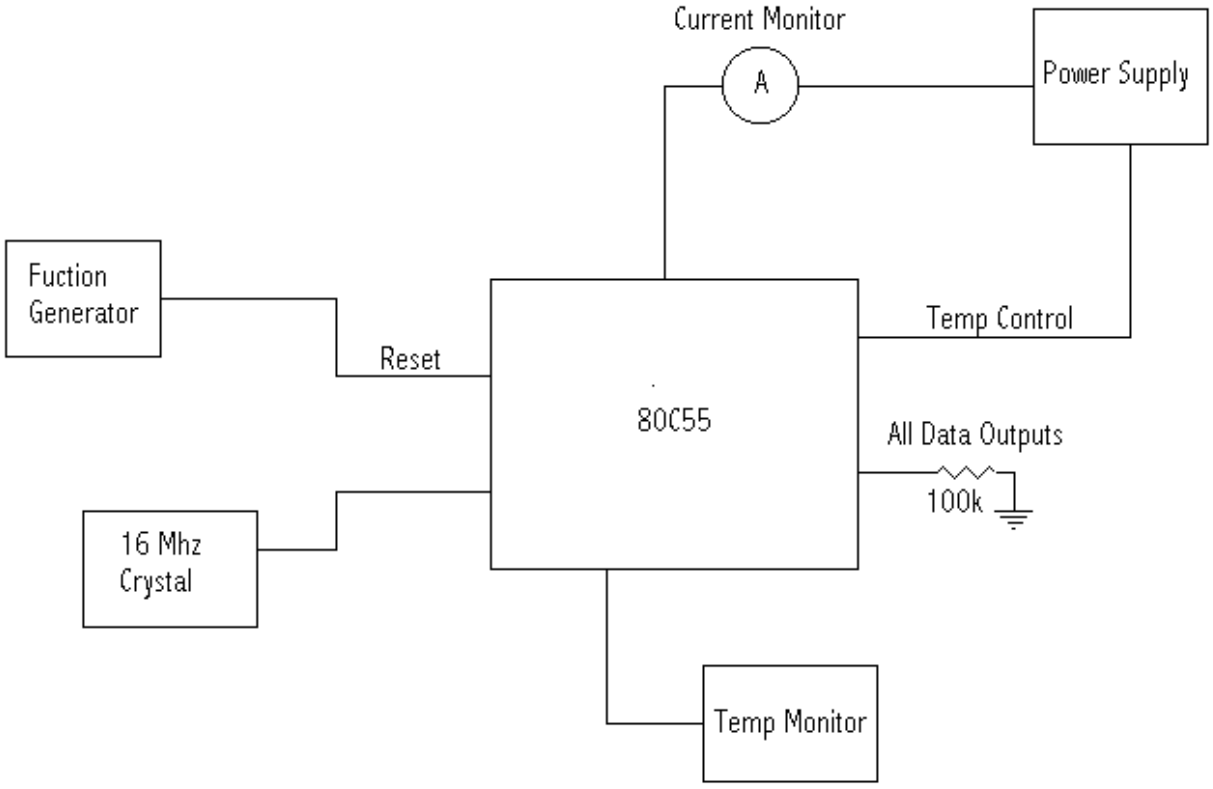

Figure 1. Block Diagram of Test System for PCA80C522 Processor.

With the processor operating in the idle mode as defined in Figure 1, ions from the accelerator would strike the device at a predetermined angle to give a known effective LET. This exposure to the ions would continue until either a latchup would occur or 10^7 ions/cm^2 was reached on target. Upon determining that a latch did occur, the ion beam was stopped and the power to the DUT was cycled to prevent damage. The recorded fluence for the time to latch was used to calculate the latchup cross section as one over the fluence to latch. Numerous cases were run in this manner to develop the cross section as a function of effective LET.

At the end of the cross section data collection, latchup dwell testing was performed. In this test, ions were used to induce a latchup. Once the latch was initiated, the ion beam was stopped and the processor was left in the latched condition for a specified time period. After that time, the power was cycled and the processor restarted and checked for nominal operation (no excessive or minimal power draw, no functionality testing was possible with the minimal test setup). The amount of time the DUT remained in the latched condition was increased in consecutive test cases until the time period was reached after which the DUT no longer resumed nominal operations.

It must be emphasized that the sample size for this test was one part. With the Phillips processor being classified as a commercial part, this data must be used with extreme caution as substantial error bars can exist for this data, including destructive latchup with zero dwell time.

V. Results

One PCA80C522 Phillips Processor device was used throughout this testing. For each of the test runs, the device was biased with 5 volts and run at 16 MHz in the idle mode. For all ions used, single event latchup was observed. The cross section data for this part as a function of Effective LET is shown in Figure 2. Latchup currents measured varied from approximately 13 to 90 mA, where nominal current was approximately 300 μA in the idle mode.

From this cross section data the LET threshold for latchup is approximately 3-5 MeV-cm^2/mg and the saturation cross section is approximately 3×10^{-3} cm^{-2} or higher. The "or higher" comment comes from the fact that the data taken at the three highest LET points was limited due to the particle flux rates achievable (BNL was not able to provide a consistent ion bean with a flux of less than approximately 250 ions/cm^2/sec). Hence, these measured cross-sections are LOWER than the actual cross-sections.

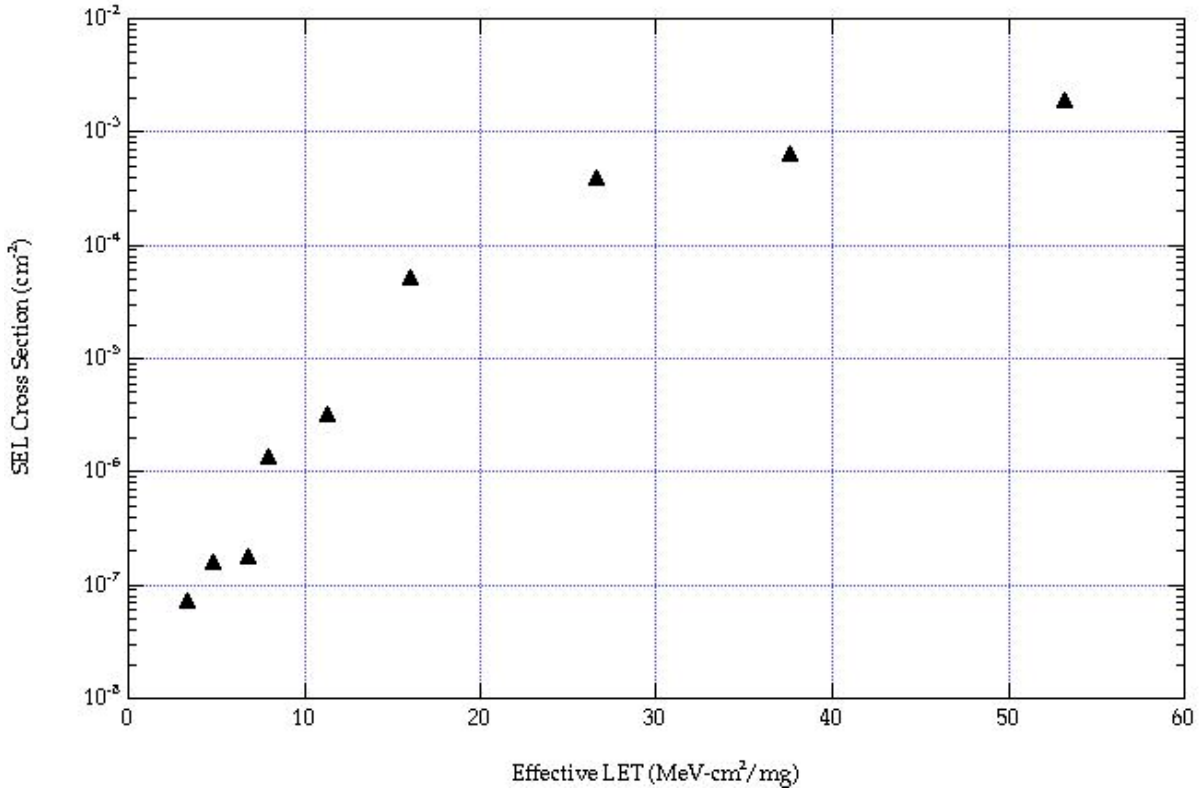

Figure 2. Cross section versus Effective LET for the PCA80C522 Phillips Processor.

It should also be noted that numerous events were observed that required a reset to the 80C552 rather than a power cycle. These single event functional interrupts (SEFIs) are not noted in Figure 2 and were not gathered except to note that they occurred. The device was approximately 5-10 times more sensitive to SEFIs than to latchup.

The second part of the testing was the dwell test. This data is summarized in Table I. Dwell times of 5, 10, 15, 30 and 60 seconds were used for this testing. For each of these cases, the latchup current was at whatever level occurred (no effort was made to chose the current level for the dwell testing). For the first four time intervals, the processor

after having its power cycled resumed nominal operation. However, after latching and being allowed to stay in the latched state for 60 seconds, a power cycle would not recover to nominal operation (current draw stayed in excess of 15 mA). No number of power cycles or power off times were able to recover the DUT to nominal operation. Therefore, the latchup that occurs in these devices does become destructive if allowed to stay latched for a time in excess of 30 seconds.

Table I

SEL current in mA	Time in seconds of dwell	Recovery?
90	5	yes
58	10	yes
60	15	yes
84	30	yes
26	60	**NO, hard failure of device**

VI. Summary

The PCA80C522 Phillips Processor was exposed to ions with LETs ranging from approximately 3 to 26 MeV-cm^2/mg. Latchup was observed for all ions used (but at the lowest LET not all runs produced latches). Based on this, PCA80C522 Phillips Processors are susceptible to single event induced latchup, and the LET threshold for this event is approximately 3-5 MeV-cm^2/mg and has a saturation cross section of approximately 3×10^{-3} cm^{-2} or higher. The latchup that occurs in these devices does become destructive if allowed to stay latched for a time in excess of 30 seconds.

VII. Recommendations

In general, devices are categorized based on heavy ion test data into one of the four following categories:

Category 1 – Recommended for usage in all NASA/GSFC spaceflight applications.
Category 2 – Recommended for usage in NASA/GSFC spaceflight applications, but may require mitigation techniques.
Category 3 – Recommended for usage in some NASA/GSFC spaceflight applications, but requires extensive mitigation techniques or hard failure recovery mode.
Category 4 – Not recommended for usage in any NASA/GSFC spaceflight applications.

The PCA80C522 Phillips Processors are Category 3 devices.